REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested. Since the present Response raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested under the provisions of 37 C.F.R. §1.116.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants submit that Claim 49 is not directed to a non-elected invention. It is the Examiner's position that Claim 49 is distinct for reciting that "partially decomposing occurs during ferroelectric deposition, top electrode deposition, optional encapsulate deposition, BEOL process or device operation so as to release oxygen into the ferroelectric capacitor." Applicants note that the above passage was the subject matter of the original dependent Claim 46 that is now rewritten as independent Claim 49 including the limitations of base Claim 31. Claim 49 is not independent and distinct from the originally claimed invention because independent Claim 49 includes all the limitations of independent Claim 31 and is further limited with the subject matter of a previously examined dependent claim. Applicants respectfully request that Claim 49 be examined on the merits.

Now turning to the rejections of the present Final Action, Claims 31-38, 40-42, 45, and 47 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over the publication to Robert E. Jones Jr., *Ferroelectric Nonvolative Memories for Embedded Applications*, IEEE Custom Integrated Circuits Conference (1988)("Jones Jr., et al.")[1] in view of U.S. Patent No. 6,015,989 to Horikawa, et al. ("Horikawa, et al."). Claims 43-44 stand rejected under 35

[1] Applicants observe that in the Final Rejection the Examiner cites U.S. Patent No. 5,716,975. The '975 patent relates to compounds useful as hypoglycemic agents and for treating Alzheimer's disease. The above citation of Jones, Jr. is correct.

U.S.C. §103(a), as allegedly obvious over the combination of Jones Jr., et al., Horikawa, et al., and U.S. Patent No. 6,322,849 to Joshi, et al. ("Joshi, et al.").

Applicants provide a ferroelectric (FE) capacitor and a method of fabricating the same. More specifically, the present invention relates to a method of fabricating an integrated ferroelectric/CMOS structure comprising the steps of: forming at least one complementary metal oxide semiconductor (CMOS) device on a semiconductor wafer; forming a ferroelectric capacitor over said CMOS device, where the ferroelectric capacitor comprising at least a ferroelectric layer 22 and an oxygen source layer 26 in proximity to a conductive electrode layer 20, where said oxygen source layer 26 is a metal oxide having the formula MO_x, *where M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3*, and is capable of at least partially decomposing at temperatures below 700°C; then forming wiring levels 32 on the ferroelectric capacitor at temperatures below 450°C; and annealing the structure at a temperature between 300°C and 700°C so as to at least partially decompose the oxygen source layer to release oxygen into the ferroelectric capacitor. *The atomic percent of oxygen in the oxygen source layer, having the formula MO_x where x is from about 0.03 to about 3, is from about 1.5% to about 25%.*

Applicants submit that the applied references do not render the claims of the present application obvious because the applied references fail to teach or suggest applicants' claimed method which includes the step of "forming a ferroelectric capacitor over said CMOS device, said ferroelectric capacitor comprising at least a ferroelectric layer and an oxygen source layer in proximity to a conductive electrode layer, *where said oxygen source layer is a metal oxide having the formula MO_x, wherein M is a noble metal, a non-noble metal or mixtures and*

alloys thereof and x is from about 0.03 to about 3, and is capable of at least partially decomposing at temperatures below 700°C", as recited in Claim 31.

Jones Jr., et al., fail to teach or suggest a method including the step of depositing a oxygen source layer, where the oxygen source layer is a metal oxide having the formula MO_x, where x is from about 0.03 to about 3. Applicants note that the Examiner has admitted in the present Office Action that, "Jones Jr., et al., does not specifically show forming the oxygen source layer in proximity to a conductive electrode layer and releasing oxygen from the oxygen source layer". Therefore, since Jones Jr., et al. fail to teach or suggest an oxygen source layer, the principal reference also fail to teach or suggest that the oxygen source layer is a metal oxide having the formula MO_x, where x is from about 0.03 to about 3, as recited in Claim 31 of the present application.

Horikawa, et al. fail to fulfill the deficiencies of Jones Jr., et al. since the applied secondary reference also fails to teach or suggest a method which forms the claimed oxygen source layer having the *formula MO_x, where x is from about 0.03 to about 3*. Horikawa, et al. disclose a semiconductor device having a lower capacitor electrode 130 connected electrically with the major surface of the semiconductor substrate 101 through the connecting member 110a; a capacitor dielectric film 115 formed on the lower capacitor electrode 130; an upper capacitor electrode 116 formed on the capacitor dielectric film 115; and a second interlayer insulating film 117 formed on the capacitor upper electrode 116. The lower capacitor electrode 130 is made of a principal component selected from the group consisting of ruthenium and iridium and contains oxygen in a quantity of 0.001 to 0.1% by atomic weight %.

Horiwaka, et al. fail to teach forming an oxygen source layer having the formula MO_x, where x is from about .03 to about 3, because the oxygen concentration of the lower capacitor

electrode disclosed in the Horiwaka, et al., is not within the oxygen concentration of applicants' oxygen source layer. In the claimed method, the source layer has the formula MO_x where x ranges from 0.03 to 3. This correlates to an oxygen content of from about 1.5 to about 25 atomic %. The lower capacitor electrode 130 disclosed in Horiwaka, et al. contains oxygen in a quantity of 0.001 to 0.1% by atomic weight %. Horiwaka, et al. thus provide a structure in which the oxygen content is over an order of magnitude lower than the oxygen content in the claimed method. Therefore, Horiwaka, et al. fail to teach or suggest a method step of forming a ferroelectric capacitor over said CMOS device, said ferroelectric capacitor comprising at least a ferroelectric layer and an oxygen source layer in proximity to a conductive electrode layer, *where said oxygen source layer is a metal oxide having the formula MO_x, wherein M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3*, and is capable of at least partially decomposing at temperatures below 700°C", as recited in Claim 31.

Applicants note that Horiwaka, et al. make a single reference to a lower capacitor electrode having an oxygen concentration of about 2% *during initial anneal process steps*. See Column 9, lines 24-37. Applicants submit that this reference is to an intermediate process step, where ultimately the lower capacitor electrode is further annealed until the oxygen concentration of the lower capacitor electrode is within the desired range of 0.001 to 0.1 atomic %. Referring to Column 9, lines 24-35, Horiwaka, et al. disclose that:

> "annealing under the oxygen atmosphere for 120 minutes at 400°C to 600°C has resulted in diffusion of oxygen into the iridium thin film to allow the latter to contain oxygen in a quality of about 2%. *When the subsequent annealing at 400°C to 600°C for 60 minutes results in release of oxygen from the iridium thin film to reduce the oxygen content in the iridium thin film to thereby control the oxygen content to a desired value, that is within the range of .001 to .1%.* In this way, the oxygen content in the iridium film can be controlled to the desired value by effecting the

annealing after formation of the iridium film forming the lower capacitor electrode."

"It is impermissible within the framework of §103 to pick and choose from any one reference only as much of it as well support a give position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggest to one of ordinary skill in the art". *In re Wesslau*, 147 U.S.P.Q. 391, 393 (1965). Therefore, Horiwaka, et al. do not teach or suggest forming an oxygen source layer is a metal oxide having the formula MO_x, where x is from about 0.03 to about 3.

Applicants further submit that Horiwaka, et al. teach away from the present invention. Horiwaka, et al. disclose that a low concentration of oxygen in the lower capacitor electrode suppresses the diffusion of Si in order to reduce the formation of a silicide on the lower electrode. Horiwaka, et al., referring to Column 8, lines 10-36, further disclose that it is disadvantageous, "if the oxygen content in the ruthenium thin-film is increased to a value not lower than 0.05%, it appears that the use of the annealing temperature of 650°C may result in *increase of the contact resistance* by 2 to 3 units. This appears because the oxygen added to the ruthenium thin-film *becomes excessive*". A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore and Associates, Inc. v. Garlock, Inc.,* 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Therefore, Horiwaka, et al. teach away from applicants' claimed method as recited in Claim 31.

Joshi, et al. also fail to fulfill the deficiencies of the applied prior art. More specifically, Joshi, et al. do not teach or suggest forming an oxygen source layer having the formula MO_x, where x is from about 0.03 to about 3. Joshi, et al. provide a method for

fabricating a ferroelectric integrated circuit that reduces or eliminates the degradation of electronic properties resulting from exposure to hydrogen. Joshi, et al., referring to FIG. 1, disclose a ferroelectric capacitor 118 comprising a bottom electrode 120 made of platinum and having a thickness of 2000Å, a ferroelectric thin film 122 formed on the bottom electrode 120, and a top electrode 124 formed on the ferroelectric film 122, made of platinum and having a thickness of 2000 Å. Joshi, et al. do not teach or suggest a method including the step of "forming a ferroelectric capacitor over said CMOS device, said ferroelectric capacitor comprising at least a ferroelectric layer and *an oxygen source layer* in proximity to a conductive electrode layer, where said *oxygen source layer is a metal oxide having the formula* MO_x, *wherein M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3"* as recited in Claim 31.

In addition to failing to teach or suggest internal oxygen source layer, Joshi, et al. teach away from utilizing an oxygen annealing ambient. Joshi, et al. disclose high temperature oxygen annealing disadvantageously generates defects in silicon crystalline structures. *See* Column 2, lines 20-27. Joshi, et al. further disclose that eliminating high temperature O_2 recovery annealing and utilizing a high temperature inert gas recovery anneal advantageously reverses the effects of hydrogen degradation. *See* Column 2, lines 55-63. Therefore, since Joshi, et al. fail to disclose an oxygen source layer and teaches away from utilizing an annealing ambient that comprises oxygen, Joshi, et al. lead away from applicants' claimed method as recited in Claim 31.

The §103 rejections also fail because there is no motivation in the applied references which suggests modifying the disclosed methods and structures to include the various features, particularly the claimed method including forming a ferroelectric capacitor over said

CMOS device, said ferroelectric capacitor comprising at least a ferroelectric layer and an oxygen source layer in proximity to a conductive electrode layer, *where said oxygen source layer is a metal oxide having the formula MO_x, wherein M is a noble metal, a non-noble metal or mixtures and alloys thereof and x is from about 0.03 to about 3.* Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Vaeck*, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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